REMARKS

The rejections presented in the Office Action dated August 25, 2005 have been considered. Claims 1-14 are pending in the application. Claims 2-5, 10, and 12-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No amendments are made because the independent claims are understood to be novel over Waters. Reconsideration and allowance of the application are respectfully requested.

The Office Action fails to show that Claims 1, 6, 7, 8, 9 and 11 are anticipated by US patent application no. 2004/0143801 to Waters et al. ("Waters") under 35 USC §102(e). The rejection is respectfully traversed because the Office Action fails to show that all the limitations of the claims are taught by Waters.

The Office Action fails to consider all the limitations in alleging that Waters anticipates Claim 1. For example, Claim 1 limitations include simulating behavior of the system-level design consistent with the system-level functions and behavior of a hardware definition from the hardware-level design objects that implement the user-selected ones of the system-level design objects. The Office Action cites Waters' columns [0148]-[0185] as teaching the limitations of simulating behavior of the system-level design consistent with the system-level functions but does not cite any teachings of Waters as teaching that the simulation is also consistent with the behavior of a hardware definition from the hardware-level design objects that implement the user-selected ones of the system-level design objects. Furthermore, Waters' paragraphs [0148]-[0185] appear to teach that the system-level simulation is independent of the hardware-level design objects.

Specifically, Waters' paragraph [0152] – [0155] teach that the system design is simulated with a C++ executable which "provides feedback about algorithmic behavior of the C++ class early in the design process." [0155]. "As long as specification and simulation is at the algorithmic level, handshaking code controlling when data should be passed to and from the design unit is not needed." [0037]. Thus, Waters' simulation of the algorithmic design is independent of and not performed consistent

with behavior of any hardware-level design objects.

The Office Action also fails to show that Waters teaches the limitations of each hardware-level design object configured to generate a hardware definition of a hardware-level function, wherein one or more hardware-level design objects are combinable to implement each system-level design object. The cited paragraphs [0135]-[0144] teach that Waters' design tool translates the C++ hierarchical objects into an HDL description. Thus, Waters' design tool apparently translates the C++ hierarchy into HDL, and there are no apparent hardware-level design objects configured to generate a hardware definition as claimed. An explanation is requested as to the specific elements of Waters thought to correspond to the claimed hardware-level design objects if the rejection is maintained.

The limitations of claims 6-8 are not shown to be taught by Waters. For example, claim 6 sets forth a particular method for generating a testbench, and Waters is not shown to teach the claimed method. Claim 6 includes limitations of simulating behavior of the design defined in the system-level design file with user-specified input-data generators that generate system-level input data; capturing the system-level input data generated by the input-data generators; and generating a hardware definition for a first testbench component that provides the system-level input data as input data to the hardware definitions. It is not apparent how Waters is construed to teach this manner of generating a test bench, when Waters clearly teaches simulation "with pre-existing HDL IP code in a test bench" (para. [0157]). Thus, the Office Action fails to show that Waters teaches the limitations of claims 6-8.

Claim 9 is an apparatus claim, and Claim 11 is a system claim, both including functional limitations similar to those of claim 1. Therefore, claims 9 and 11 are not shown to be anticipated Waters.

The rejection of Claims 1, 6, 7, 8, 9, and 11 as being anticipated by Waters should be withdrawn because all the limitations of the claims are not shown to be taught by Waters.

CONCLUSION

Reconsideration and a notice of allowance are respectfully requested in view of the Amendments and Remarks presented above. If the Examiner has any questions or concerns, a telephone call to the undersigned is invited.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia, 22313-1450, on November 21, 2005.

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